August 1996, Rev D
FN7161

Video Gain Control/Fader/Multiplexer

The EL4095 is a versatile variable-gain building block. At its core is a fader which can variably blend two inputs together and an output amplifier that can drive heavy loads. Each input appears as the input of a current-feedback amplifier and with external resistors can separately provide any gain desired. The output is defined as:

$V_{OUT} = A*V_{INA}$ (0. 5V + V_{GAIN}) + B*V_{INB} (0.5V–V_{GAIN}),

where A and B are the fed-back gains of each channel.

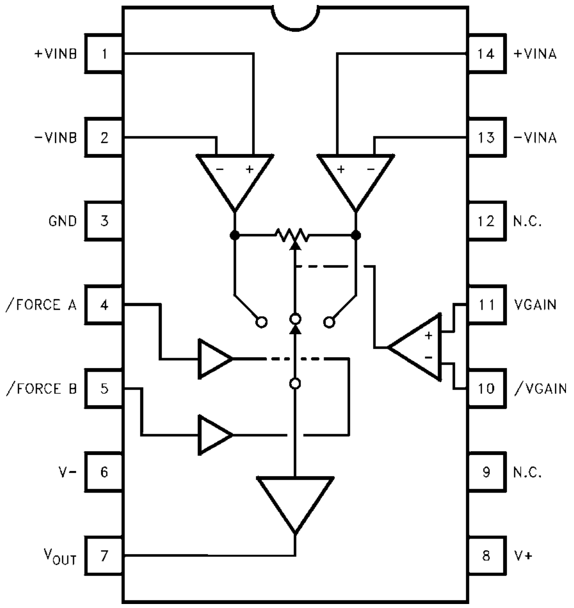
Additionally, two logic inputs are provided which each override the analog V_{GAIN} control and force 100% gain for one input and 0% for the other. The logic inputs switch in only 25ns and provide high attenuation to the off channel, while generating very small glitches.

Signal bandwidth is 60MHz, and gain-control bandwidth 20MHz. The gain control recovers from overdrive in only 70ns.

The EL4095 operates from ±5V to ±15V power supplies, and is available in both 14-pin DIP and narrow surface mount packages.

Pinout

EL4095
(14-PIN PDIP, SO)
TOP VIEW



Manufactured under U.S. Patent No. 5,321,371, 5,374,898

Features

- Full function video fader
- 0.02%/0.02° differential gain/phase @ 100% gain
- 25ns multiplexer included
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60MHz bandwidth
- Low thermal errors

Applications

- Video faders/wipers
- Gain control
- Graphics overlay
- Video text insertion
- Level adjust
- Modulation

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4095CN	-40°C to +85°C	14-Pin PDIP	MDP0031
EL4095CS	-40°C to +85°C	14-Pin SO	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

V_S+	Supply Voltage	+18V
V_S	Voltage between V_S+ and V_S-	+33V
+V_{INA},	Input Voltage	(V_S-) -0.3V
+V_{INB}		to (V_S+) +0.3V
I_{IN}	Current Into -V_{INA}, -V_{INB}	5mA
V_{GAIN}	Input Voltage	$\overline{V_{GAIN}}$ ±5V
$\overline{V_{GAIN}}$	Input Voltage	V_S- to V_S+

V_{FORCE}	Input Voltage	-1V to +6V
I_{OUT}	Output Current	±35mA
T_A	Operating Temperature Range	-40°C to +85°C
T_J	Operating Junction Temperature	0°C to +150°C
T_{ST}	Storage Temperature Range	-65°C to +150°C
	Internal Power Dissipation	See Curves

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

V_S = ±15V, T_A = 25°C, $\overline{V_{GAIN}}$ ground unless otherwise specified

PARAMETER	DESCRIPTION	LIMITS			UNITS
		MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		1.5	5	mV
I_B+	+V_{IN} Input Bias Current		5	10	µA
I_B-	-V_{IN} Input Bias Current		10	50	µA
CMRR	Common Mode Rejection	65	80		dB
-CMRR	-V_{IN} Input Bias Current Common Mode Rejection		0.5	1.5	µA/V
PSRR	Power Supply Rejection Ratio	65	95		dB
-IPSR	-V_{IN} Input Current Power Supply Rejection Ratio		0.2	2	µA/V
R_{OL}	Transimpedance	0.2	0.4		MΩ
R_{IN-}	-V_{IN} Input Resistance		80		Ω
V_{IN}	+V_{IN} Range	(V-) + 3.5		(V+) -3.5	V
V_O	Output Voltage Swing	(V-) +2		(V+) -2	V
I_{SC}	Output Short-Circuit Current	80	125	160	mA
V_{IH}	Input High Threshold at Force A or Force B Inputs			2.0	V
V_{IL}	Input Low Threshold at Force A or Force B Inputs	0.8			V
I_{FORCE}, High	Input Current of Force A or Force B, V_{FORCE} = 5V			-50	µA
I_{FORCE}, Low	Input Current of Force A or Force B, V_{FORCE} = 0V		-440	-650	µA
Feedthrough, Forced	Feedthrough of Deselected Input to Output, Deselected Input at 100% Gain Control	60	75		dB
V_{GAIN}, 100%	Minimum Voltage at V_{GAIN} for 100% Gain	0.45	0.5	0.55	V
V_{GAIN}, 0%	Maximum Voltage at V_{GAIN} for 0% Gain	-0.55	-0.5	-0.45	V
NL, Gain	Gain Control Non-linearity, V_{IN} = ±0.5V		2	4	%
R_{IN}, VG	Impedance between V_{GAIN} and $\overline{V_{GAIN}}$	4.5	5.5	6.5	kΩ
NL, A_V = 1 A_V = 0.5 A_V = 0.25	Signal Non-linearity, V_{IN} = ±1V, V_{GAIN} = 0.55V Signal Non-linearity, V_{IN} = ±1V, V_{GAIN} = 0V Signal Non-linearity, V_{IN} = ±1V, V_{GAIN} = -0.25V		<0.01 0.03 0.07	 0.4	% % %
I_S	Supply Current		17	21	mA

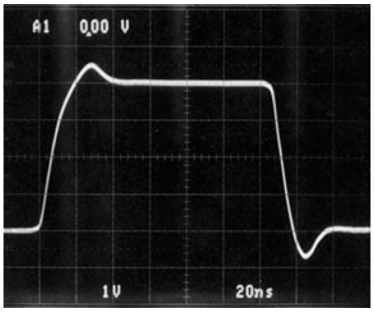
Closed-Loop AC Electrical Specifications

V_S = ±15V, A_V = +1, R_F = R_{IN} = 1kΩ, R_L = 500Ω, C_L = 15pF, C_{IN}- = 2pF, T_A = 25°C, A_V = 100% unless otherwise noted

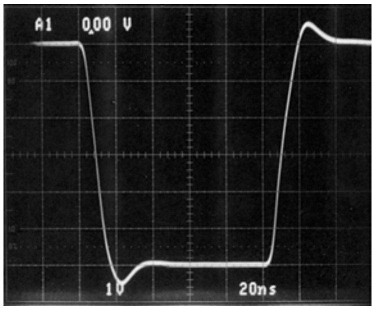
			LIMITS			
PARAMETER	**DESCRIPTION**		**MIN**	**TYP**	**MAX**	**UNITS**
SR	Slew Rate; V_{OUT} from -3V to +3V Measured at -2V and +2V			330		V/µs
BW	Bandwidth	-3dB		60		MHz
		-1dB		30		MHz
		-0.1dB		6		MHz
dG	Differential Gain; AC Amplitude of 286mV_{P-P} at 3.58MHz on DC Offset of -0.7V, 0V and +0.7V	A_V = 100%		0.02		%
		A_V = 50%		0.07		%
		A_V = 25%		0.07		%
dθ	Differential Phase; AC Amplitude of 286mV_{P-P} at 3.58MHz on DC Offset of -0.7V, 0V and +0.7V	A_V = 100%		0.02		°
		A_V = 50%		0.05		°
		A_V = 25%		0.15		°
T_S	Settling Time to 0.2%; V_{OUT} from -2V to +2V	A_V = 100%		100		ns
		A_V = 25%		100		ns
T_{FORCE}	Propagation Delay from V_{FORCE} = 1.4V to 50% Output Signal Enabled or Disabled Amplitude			25		ns
BW, Gain	-3dB Gain Control Bandwidth, V_{GAIN} Amplitude 0.5 V_{P-P}			20		MHz
T_{REC}, Gain	Gain Control Recovery from Overload; V_{GAIN} from -0.7V to 0V			70		ns

Typical Performance Curves

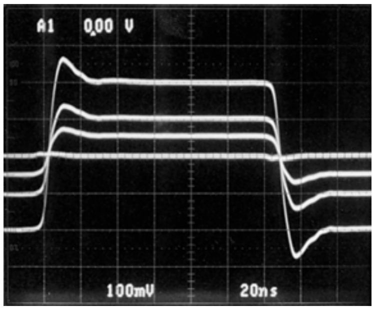
Large-Signal Pulse Response Gain = +1



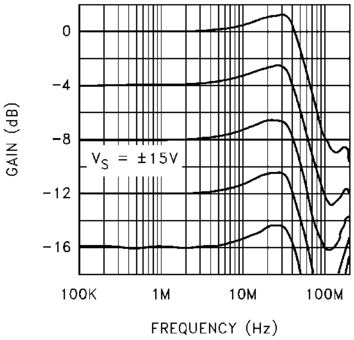
Large-Signal Pulse Response Gain = -1



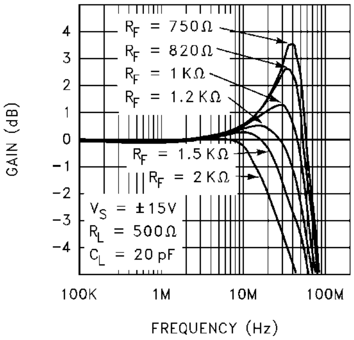
Small-Signal Pulse Response for Various Gains



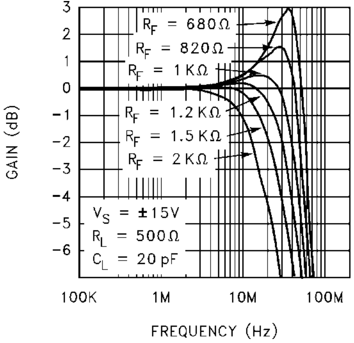
Frequency Response for Different Gains-A_V = +1



Frequency Response with Different Values of R_F - Gain = +1

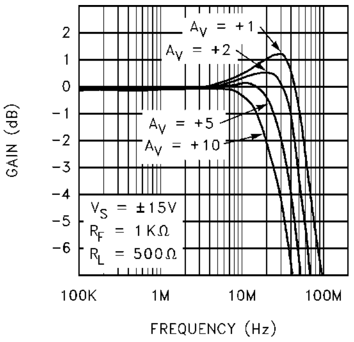


Frequency Response with Different Values of R_F - Gain = -1

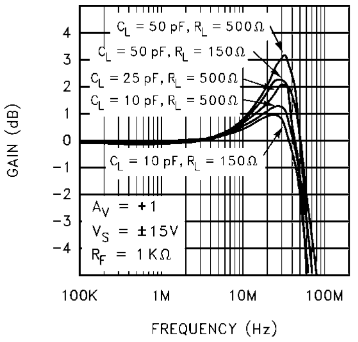


Typical Performance Curves (Continued)

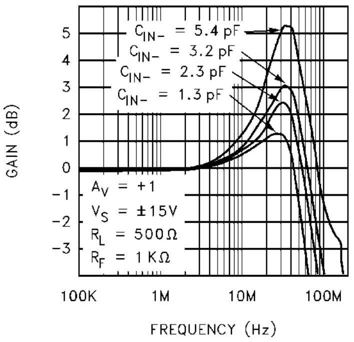
Frequency Response with Different Values of R_F - Gain = -1



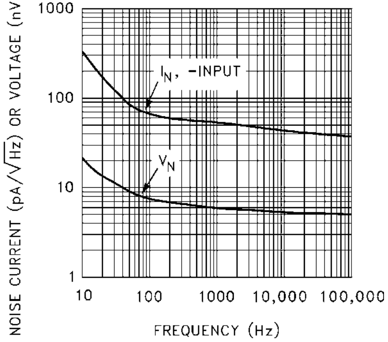
Frequency Response with Various Load Capacitances and Resistances



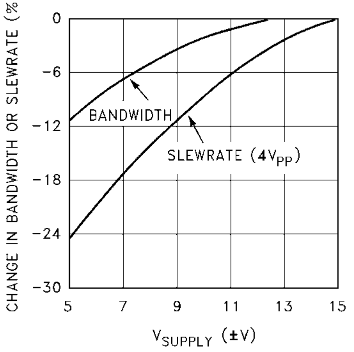
Frequency Response with Various Values of Parasitic C_{IN-}



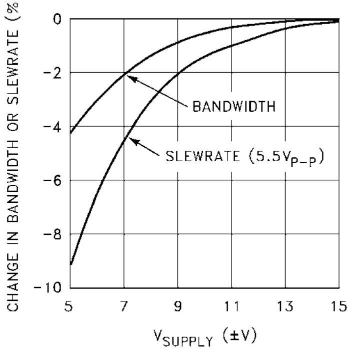
Input Noise Voltage and Current vs Frequency



Change in Bandwidth and Slewrate with Supply Voltage - Gain = +1

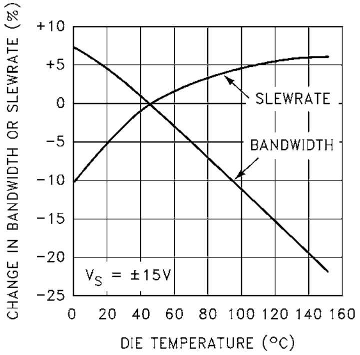


Change in Bandwidth and Slewrate with Supply Voltage - Gain = -1

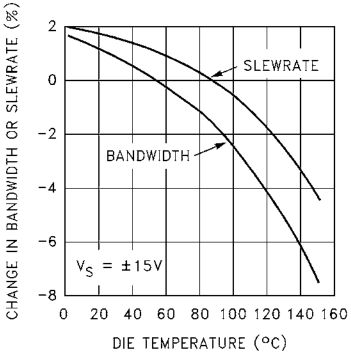


Typical Performance Curves (Continued)

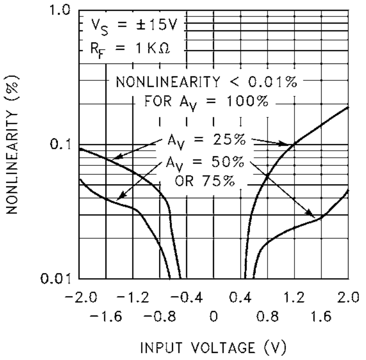
Change in Bandwidth and Slewrate with Temperature - Gain = +1



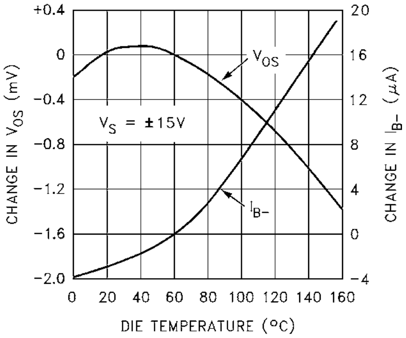
Change in Bandwidth and Slewrate with Temperature - Gain = -1



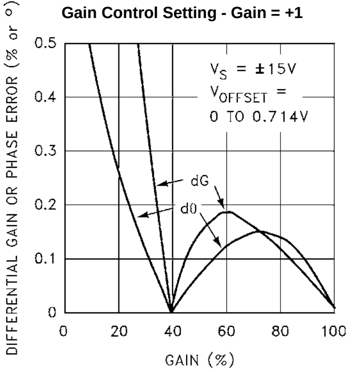
DC Nonlinearity vs Input Voltage - Gain = +1



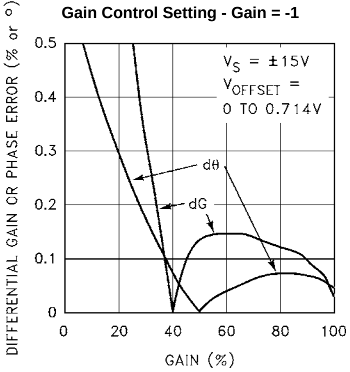
Change in V_{OS} and I_{B-} vs die Temperature



Differential Gain and Phase Errors vs Gain Control Setting - Gain = +1

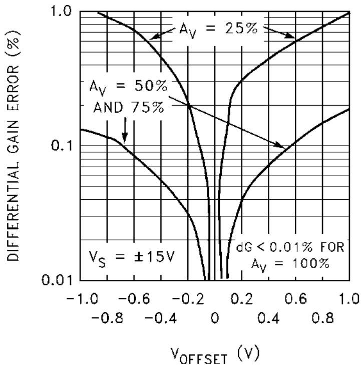


Differential Gain and Phase Errors vs Gain Control Setting - Gain = -1

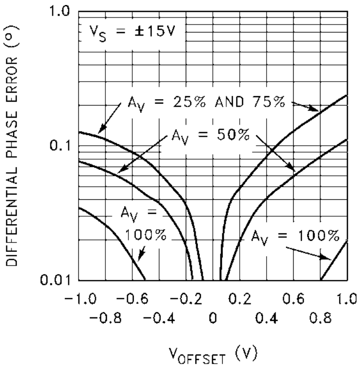


Typical Performance Curves (Continued)

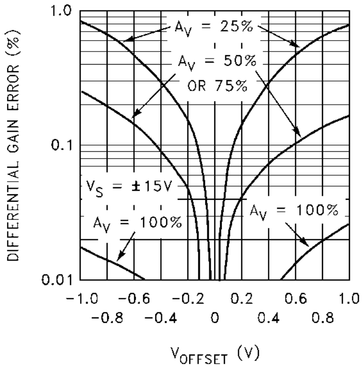
Differential Phase Error vs DC Offset - Gain = +1



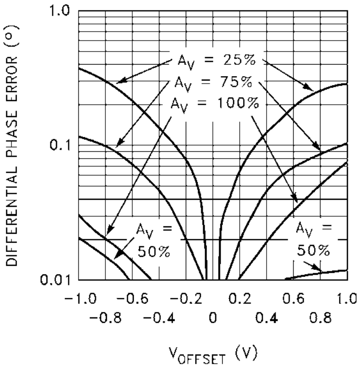
Differential Phase Error vs DC Offset - Gain = +1



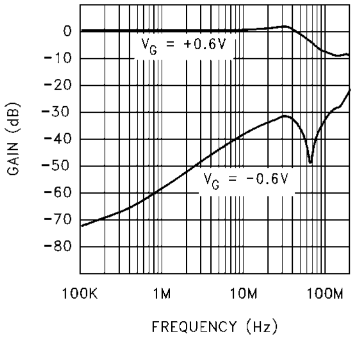
Differential Phase Error vs DC Offset - Gain = -1



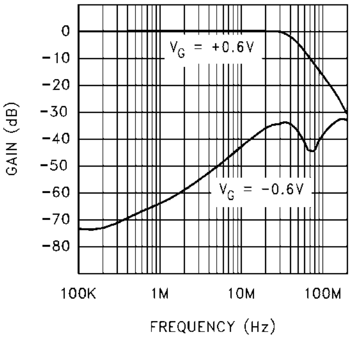
Differential Phase Error vs DC Offset - Gain = -1



Attenuation over Frequency - Gain = +1

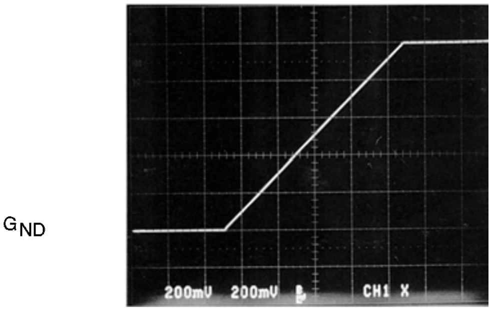


Attenuation over Frequency - Gain = -1

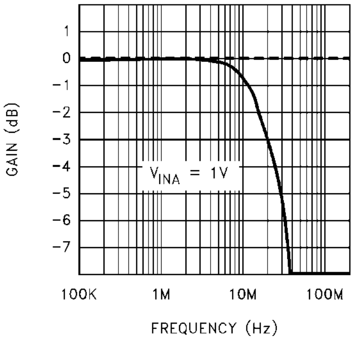


Typical Performance Curves (Continued)

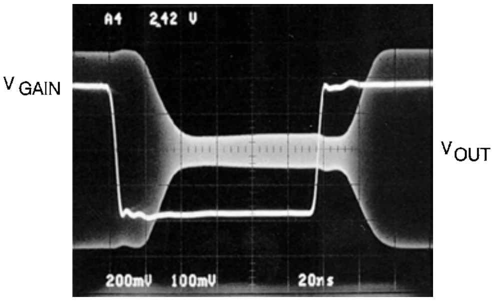
Gain vs V_G (1 V_{DC} at V_{INA})



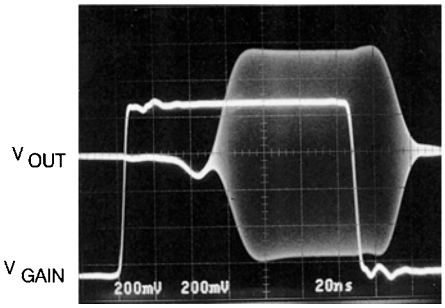
Gain Control Gain vs Frequency



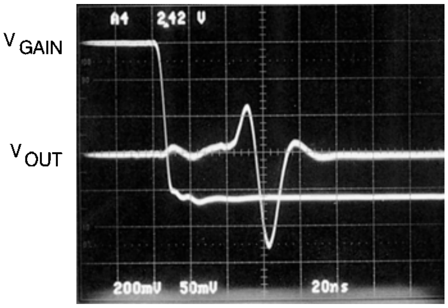
Gain Control Response to a Non-Overloading Step, Constant Sinewave at V_{INA}



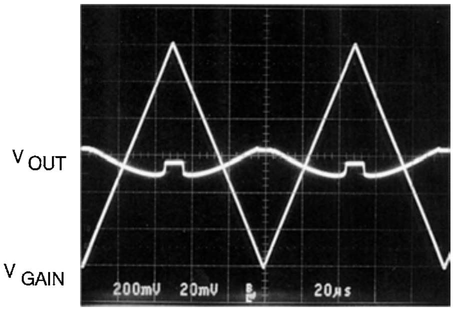
V_{GAIN} Overload Recovery Delay



V_{GAIN} Overload Recovery Response—No AC Input

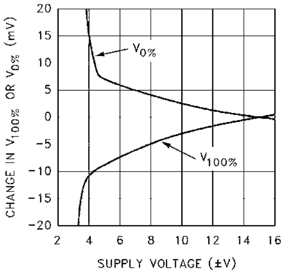


Cross-Fade Balance -0V on A_{IN} and B_{IN}; Gain = +1

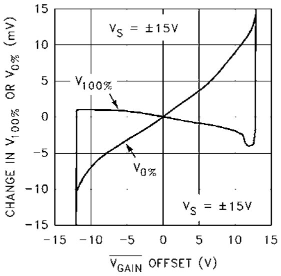


Typical Performance Curves (Continued)

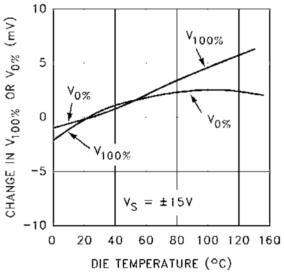
Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Supply Voltage



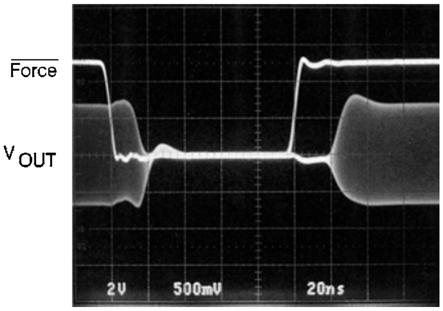
Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs $\overline{V_{GAIN}}$ Offset



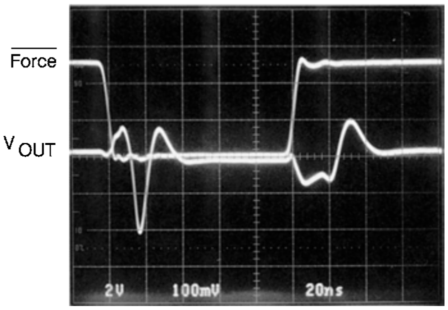
Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Die Temperature



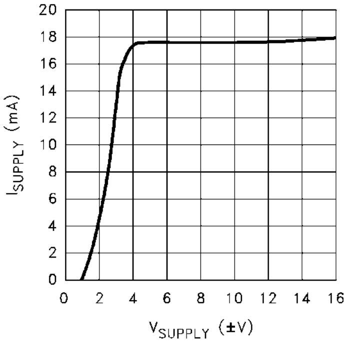
$\overline{\text{Force}}$ Response



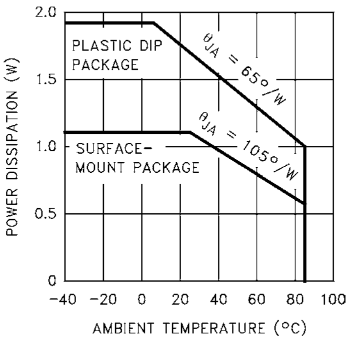
$\overline{\text{Force}}$-Induced Output Transient



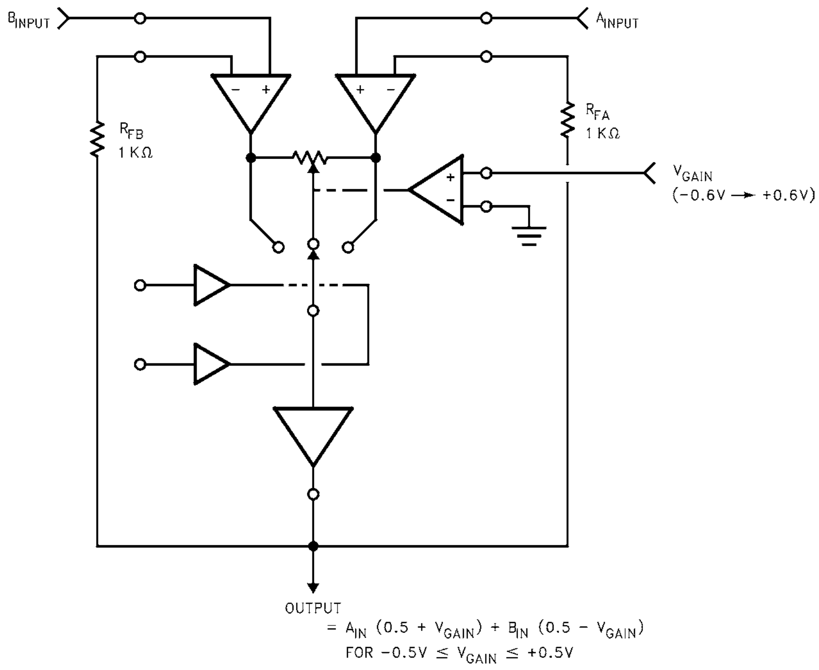
Supply Current vs Supply Voltage



Package Power Dissipation vs Ambient Temperature



Test Circuit, $A_V = +1$



Applications Information

The EL4095 is a general-purpose two-channel fader whose input channels each act as a current-feedback amplifier (CFA) input. Each input can have its own gain factor as established by external resistors. For instance, the Test Circuit shows two channels each arranged as +1 gain, with the traditional single feedback resistor R_F connected from V_{OUT} to the $-V_{IN}$ of each channel.

The EL4095 can be connected as an inverting amplifier in the same manner as any CFA.

Frequency Response

Like other CFAs, there is a recommended feedback resistor, which for this circuit is 1kΩ. The value of RF sets the closed-loop -3dB bandwidth, and has only a small range of practical variation. The user should consult the typical performance curves to find the optional value of R_F for a given circuit gain. In general, the bandwidth will decrease slightly as closed-loop gain is increased; R_F can be reduced to make up for bandwidth loss. Too small a value of R_F will cause frequency response peaking and ringing during transients. On the other hand, increasing R_F will reduce bandwidth but improve stability.

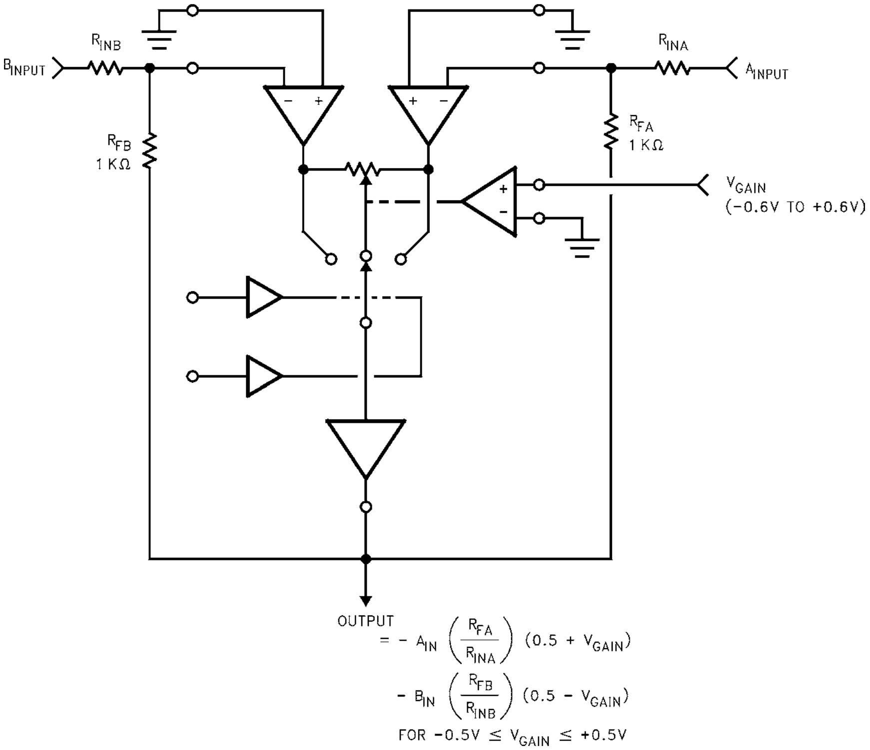


FIGURE 1. EL4095 IN INVERTING CONNECTION

Stray capacitance at each -V_{IN} terminal should absolutely be minimized, especially in a positive-gain mode, or peaking will occur. Similarly, the load capacitance should be minimized. If more than 25pF of load capacitance must be driven, a load resistor from 100Ω to 400Ω can be added in parallel with the output to reduce peaking, but some bandwidth degradation may occur. A “snubber” load can alternatively be used. This is a resistor in series with a capacitor to ground, 150Ω and 100pF being typical values. The advantage of a snubber is that it does not draw DC load current. A small series resistor, low tens of ohms, can also be used to isolate reactive loads.

Distortion

The signal voltage range of the +V_{IN} terminals is within 3.5V of either supply rail.

One must also consider the range of error currents that will be handled by the -V_{IN} terminals. Since the -V_{IN} of a CFA is the output of a buffer which replicates the voltage at +V_{IN}, error currents will flow into the -V_{IN} terminal. When an input channel has 100% gain assigned to it, only a small error current flows into its negative input; when low gain is assigned to the channel the output does not respond to the channel’s signal and large error currents flow.

Here are a few idealized examples, based on a gain of +1 for channels A and B and R_F = 1kΩ for different gain settings:

Gain	V_{INA}	V_{INB}	I (-V_{INA})	I (-V_{INB})	V_{OUT}
100%	1V	0	0	1mA	1V
75%	1V	0	-250µA	750µA	0.75V
50%	1V	0	-500µA	500µA	0.5V
25%	1V	0	-750µA	250µA	0.25V
0%	1V	0	-1mA	0	0V

Thus, either -V_{IN} can receive up to 1mA error current for 1V of input signal and 1kΩ feedback resistors. The maximum error current is 3mA for the EL4095, but 2mA is more realistic. The major contributor of distortion is the magnitude of error currents, even more important than loading effects. The performance curves show distortion versus input amplitude for different gains.

If maximum bandwidth is not required, distortion can be reduced greatly (and signal voltage range enlarged) by increasing the value of R_F and any associated gain-setting resistor.

100% Accuracies

When a channel gain is set to 100%, static and gain errors are similar to those of a simple CFA. The DC output error is expressed by

$$V_{OUT}, \text{Offset} = V_{OS} * A_V + (I_B-) * R_F$$

The input offset voltage scales with fed-back gain, but the bias current into the negative input, I_B-, adds an error not dependent on gain. Generally, I_B- dominates up to gains of about seven.

The fractional gain error is given by

$$E_{GAIN} = (R_F + A_V * R_{IN} -)\ R_F + A_V\ R_{IN})/R_{OL}$$

The gain error is about 0.3% for a gain of one, and increases only slowly for increasing gain. R_{IN}- is the input impedance of the input stage buffer, and R_{OL} is the transimpedance of the amplifier, 80kΩ and 350kΩ respectively.

Gain Control Inputs

The gain control inputs are differential and may be biased at any voltage as long as $\overline{V_{GAIN}}$ is less than 2.5V below V+ and 3V above V-. The differential input impedance is 5.5kΩ, and a common-mode impedance is more than 500kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of V_{INA} input at +0.5V of gain control voltage, and 0% at -0.5V of gain control. V_{INB}'s gain is complementary to that of V_{INA}; +0.5V of gain control sets 0% gain at V_{INB} and -0.5V gain control sets 100% V_{INB} gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10mV of "soft" transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation of 0% gain, it is necessary to overdrive the gain control input by about 30mV. This would set the gain control voltage range as -0.565mV to +0.565V, or 30mV beyond the maximum guaranteed 0% to 100% range.

In fact, the gain control internal circuitry is very complex. Here is a representation of the terminals:

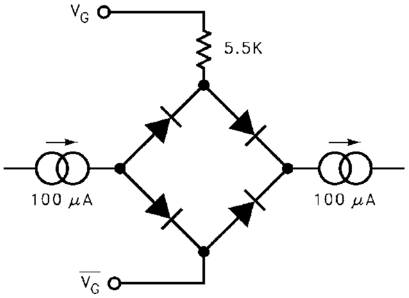


FIGURE 2. REPRESENTATION OF GAIN CONTROL INPUTS V_G AND $\overline{V_G}$

For gain control inputs between ±0.5V (±90µA), the diode bridge is a low impedance and all of the current into V_G flows back out through $\overline{V_G}$. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the V_G impedance rises sharply from the nominal 5.5kΩ to over 500kΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristics than does the simple diode bridge of this representation.

The gain input has a 20MHz -3dB bandwidth and 17ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Force Inputs

The Force inputs completely override the V_{GAIN} setting and establish maximum attainable 0% and 100% gains for the two input channels. They are activated by a TTL logic low on either of the $\overline{\text{FORCE}}$ pins, and perform the analog switching very quickly and cleanly. $\overline{\text{FORCEA}}$ causes 100% gain on the A channel and 0% on the B channel. $\overline{\text{FORCEB}}$ does the reverse, but there is no defined output state when $\overline{\text{FORCEA}}$ and $\overline{\text{FORCEB}}$ are simultaneously asserted.

The Force inputs do not incur recovery time penalties, and make ideal multiplexing controls. A typical use would be text overlay, where the A channel is a video input and the B channel is digitally created text data. The $\overline{\text{FORCEA}}$ input is set low normally to pass the video signal, but released to display overlay data. The gain control can be used to set the intensity of the digital overlay.

Other Applications Circuits

The EL4095 can also be used as a variable-gain single input amplifier. If a 0% lower gain extreme is required, one channel's input should simply be grounded. Feedback resistors must be connected to both -V_{IN} terminals; the EL4095 will not give the expected gain range when a channel is left unconnected.

This circuit gives +0.5 to +2.0 gain range, and is useful as a signal leveller, where a constant output level is regulated from a range of input amplitudes:

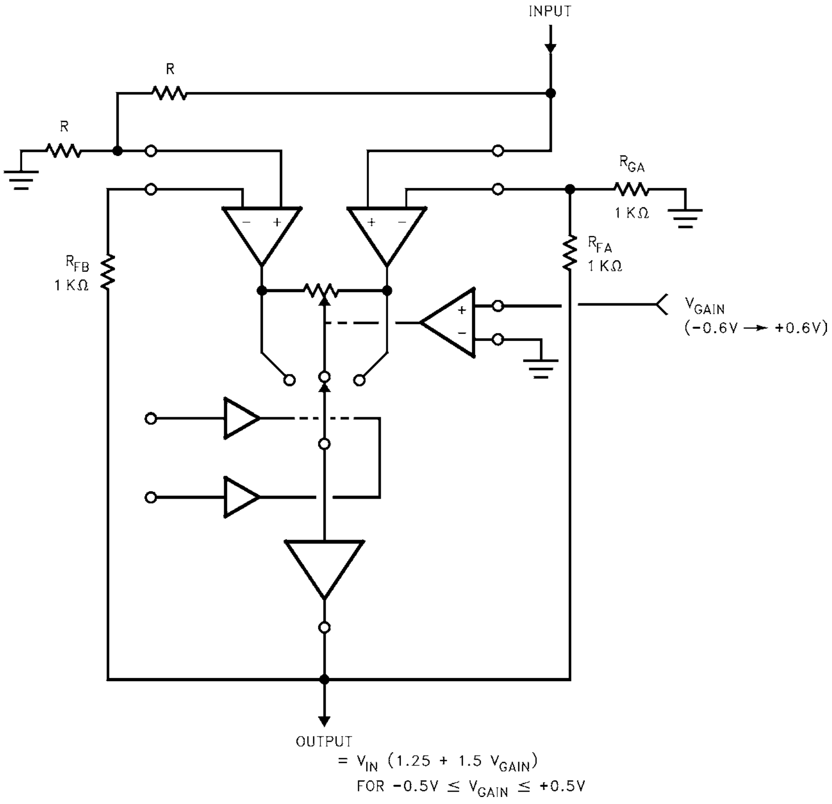


FIGURE 3. LEVELING CIRCUIT WITH 0.5 ≤ A_V ≤ 2

Here the A input channel is configured for a gain of +2 and the B channel for a gain of +1 with its input attenuated by 1/2. The connection is virtuous because the distortions do not increase monotonically with reducing gain as would the simple single-input connection.

For video levels, however, these constants can give fairly high differential gain error. The problem occurs for large inputs. Assume that a “twice-size” video input occurs. The A-side stage sees the full amplitude, but the gain would be set to 100% B-input gain to yield an overall gain of 1/2 to produce a standard video output. The $-V_{IN}$ of the A side is a buffer output that reproduces the input signal, and drives R_{GA} and R_{FA}. Into the two resistors 2.1mA of error current flows for a typical 1.4V of input DC offset, creating distortion in a A-side input stage. R_{GA} and R_{FA} could be increased together in value to reduce the error current and distortions, but increasing R_{FA} would lower bandwidth. A solution would be to simply attenuate the input signal magnitude and restore the EL4095 output level to standard level with another amplifier so:

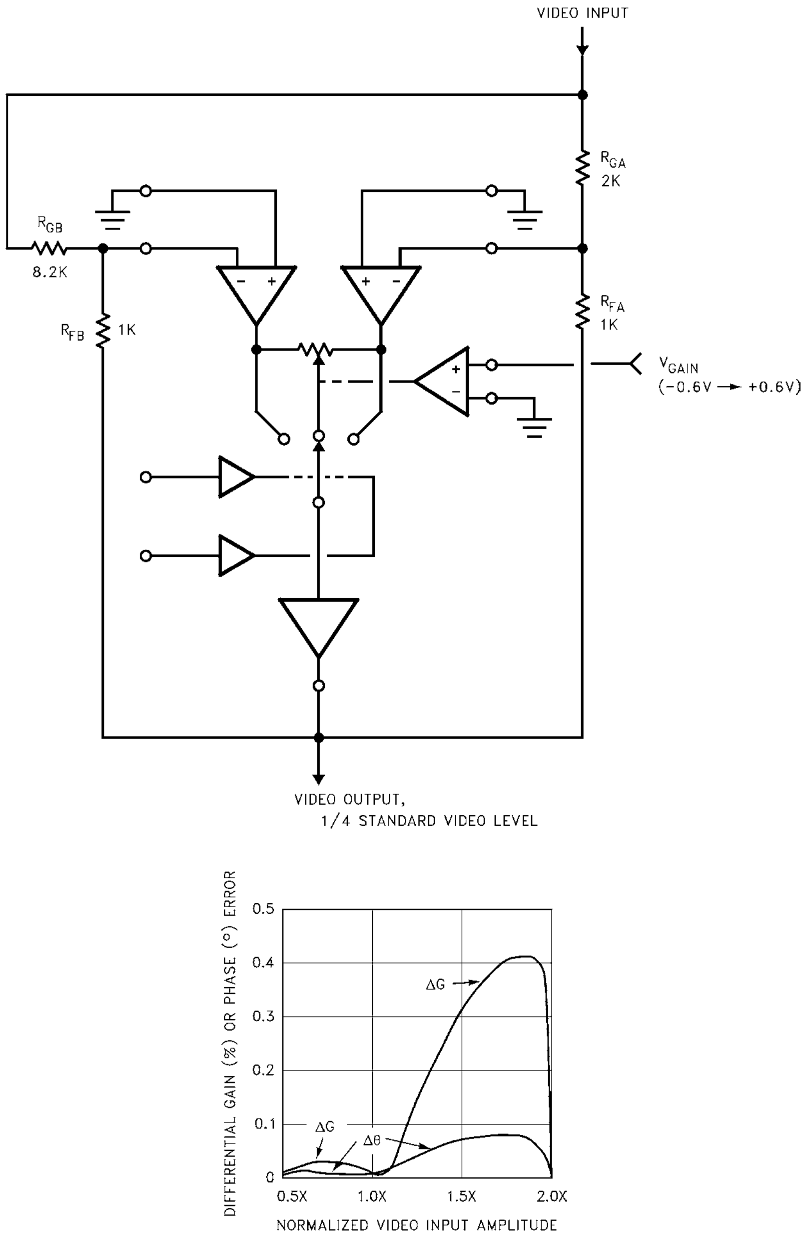


FIGURE 4. REDUCED-GAIN LEVELER FOR VIDEO INPUTS AND DIFFERENTIAL GAIN AND PHASE PERFORMANCE (SEE TEXT)

Although another amplifier is needed to gain the output back to standard level, the reduced error currents bring the differential phase error to less than 0.1 over the entire input range.

A useful technique to reduce video distortion is to DC-restore the video level going into the EL4095, and offsetting black level to -0.35V so that the entire video span encompasses ±0.35V rather than the unrestored possible span of ±0.7V (for standard-sized signals). For the preceding leveler circuit, the black level should be set more toward -0.7V to accommodate the largest input, or made to vary with the gain control itself (large gain, small offset; small gain, larger offset).

The EL4095 can be wired as a four quadrant multiplier:

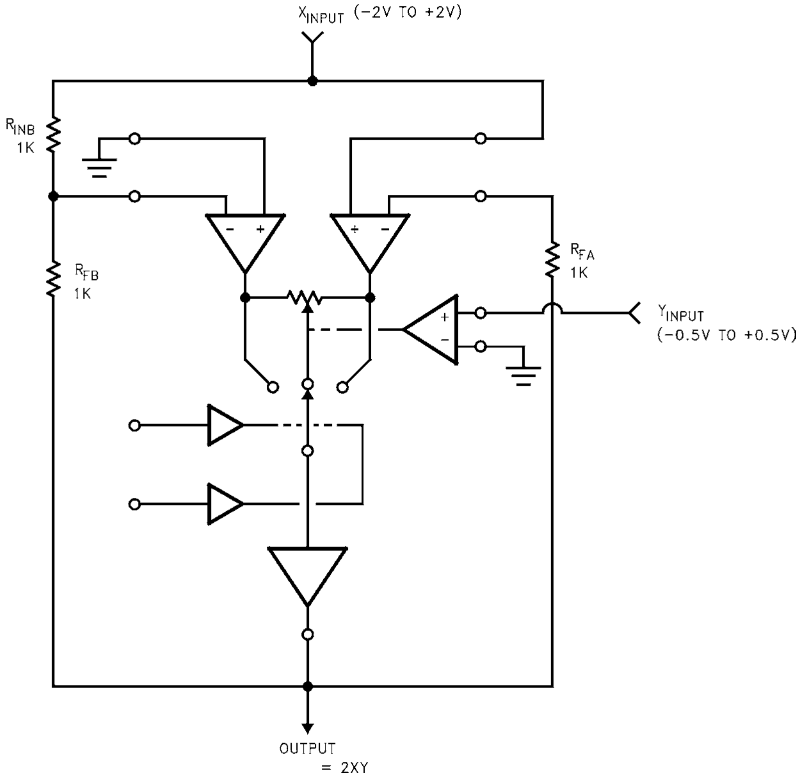


FIGURE 5. EL4095 CONNECTED AS A FOUR-QUADRANT MULTIPLIER

The A channel gains the input by +1 and the B channel by -1. Feedthrough suppression of the Y input can be optimized by introducing an offset between channel A and B. This is easily done by injecting an adjustable current into the summing junction ($-V_{IN}$ terminal) of the B input channel.

The two input channels can be connected to a common input through two dissimilar filters to create a DC-controlled variable filter. This circuit provides a controlled range of peaking through rolloff characteristics:

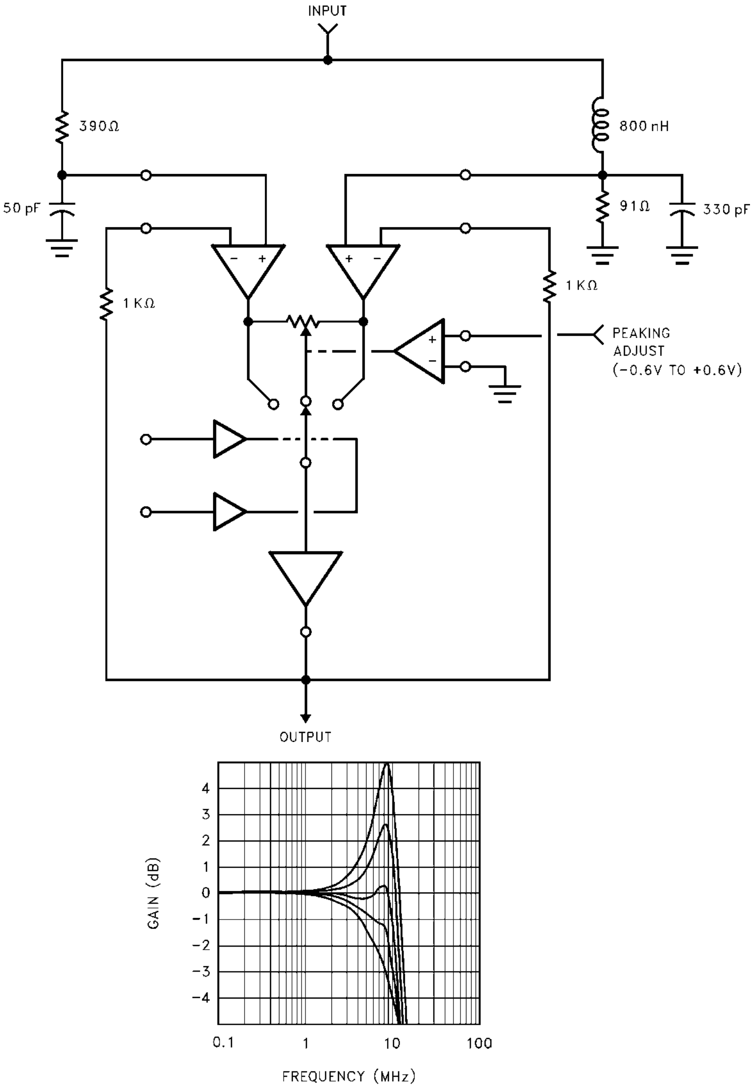


FIGURE 6. VARIABLE PEAKING FILTER

The EL4095 is connected as a unity-gain fader, with an LRC peaking network connected to the A-input and an RC rolloff network connected to the B-input. The plot shows the range of peaking controlled by the V_{GAIN} input. This circuit would be useful for flattening the frequency response of a system, or for providing equalization ahead of a lossy transmission line.

Noise

The electrical noise of the EL4095 has two components: the voltage noise in series with $+V_{IN}$ is 5nV√Hz wideband, and there is a current noise injected into $-V_{IN}$ of 35pA√Hz. The output noise will be

$$\overline{V_{n,\ out}} = \sqrt{(A_V \times \overline{V_{n,\ input}})^2 + (\overline{I_{n,\ input}} \times R_F)^2}\ ,$$

and the input-referred noise is

$$\overline{V_{n,\ input-referred}} = \sqrt{(\overline{V_{n,\ input}})^2 + (\overline{I_{n,\ input}} \times R_F / A_V)^2}$$

where A_V is the fed-back gain of the EL4095. Here is a plot of input-referred noise vs A_V:

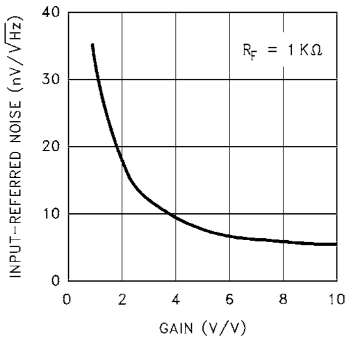


FIGURE 7. INPUT-REFERRED NOISE VS CLOSED-LOOP GAIN

Thus, for a gain of three or more the fader has a noise as good as an op-amp. The only trade-off is that the dynamic range of the input is reduced by the gain due to the nonlinearity caused by gained-up output signals.

Power Dissipation

Peak die temperature must not exceed 150°C. This allows 75°C internal temperature rise for a 75°C ambient. The EL4095 in the 14-pin PDIP package has a thermal resistance of 65°C/W, and can thus dissipate 1.15W at a 75°C ambient temperature. The device draws 20mA maximum supply current, only 600mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-14 surface-mount package has a 105°C/W thermal resistance with the EL4095, and only 714mW can be dissipated at 75°C ambient temperature. The EL4095 thus can be operated with ±15V supplies at 75°C, but additional dissipation caused by heavy loads must be considered. If this is a problem, the supplies should be reduced to ±5V to ±12V levels.

The output will survive momentary short-circuits to ground, but the large available current will overheat the die and also potentially destroy the circuit's metal traces. The EL4095 is reliable within its maximum average output currents and operating temperatures.

EL4095 Macromodel

This macromodel is offered to allow simulation of general EL4095 behavior. We have included these characteristics:

Small-signal frequency response	Signal path DC distortions
Output loading effects	V_{GAIN} I-V characteristics
Input impedance	V_{GAIN} overdrive recovery delay
Off-channel feedthrough	100% gain error
Output impedance over frequency	$\overline{\text{FORCE}}$ operation
-V_{IN} characteristics and sensitivity to parasitic capacitance	

These will give a good range of results of various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

Temperature effects	Manufacturing tolerances
Signal overload effects	Supply voltage effects
Signal and $\overline{V_G}$ operating range	Slewrate limitations
Current-limit	Noise
Video and high-frequency distortions	Power supply interactions
Glitch and delay from $\overline{\text{FORCE}}$ inputs	

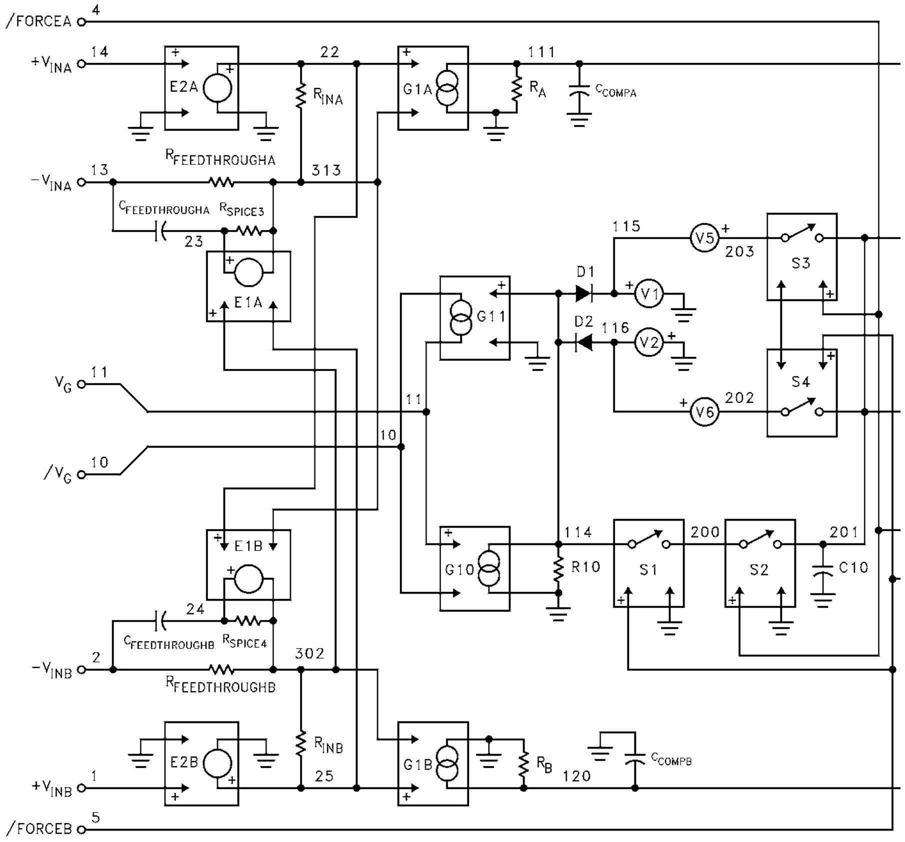
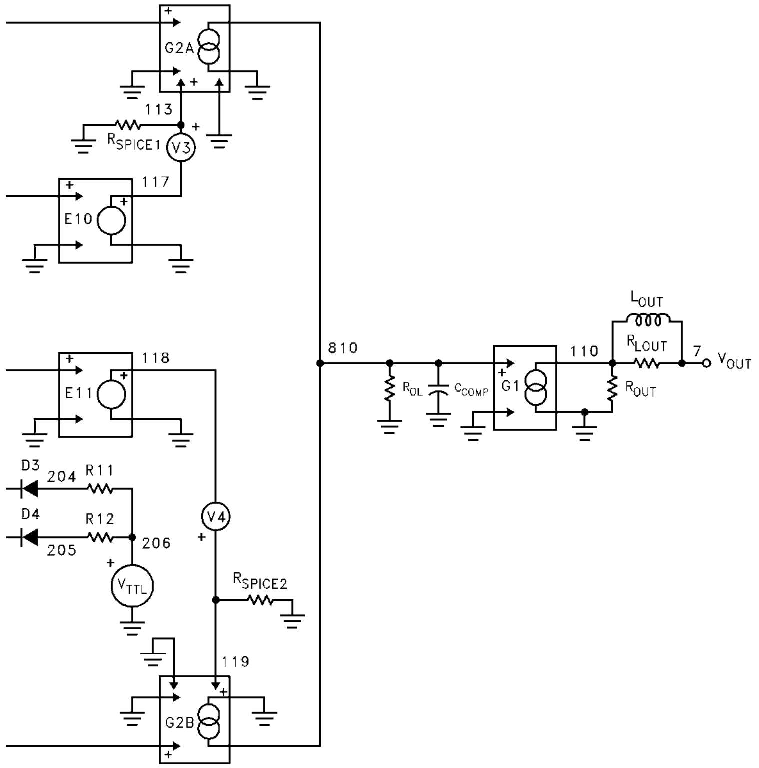


FIGURE 8. THE EL4095 MACROMODEL SCHEMATIC


G2A
113
RSPICE1
V3
117
E10
118
E11
810
LOUT
RLOUT
7
VOUT
110
ROL
CCOMP
G1
ROUT
D3
204
R11
D4
R12
205
206
VTTL
V4
RSPICE2
119
G2B